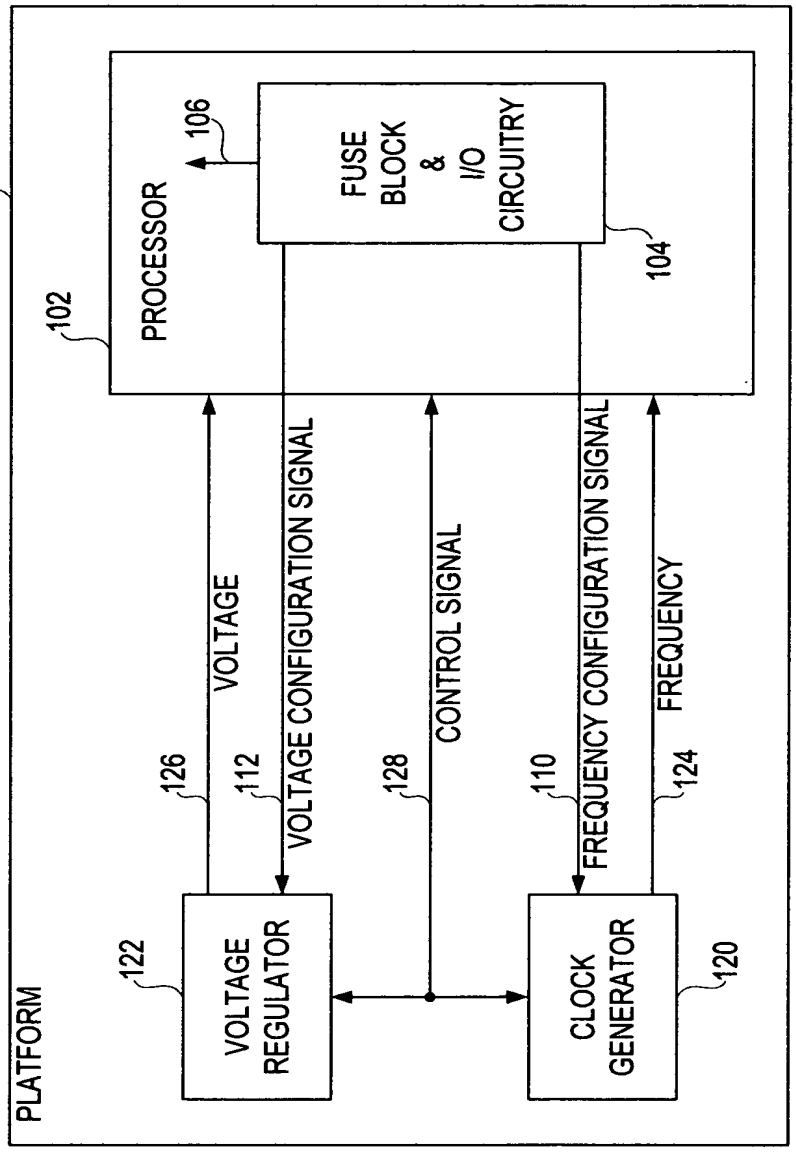
100
PLATFORM
102
PROCESSOR
106
FUSE BLOCK & I/O CIRCUITRY
104
VOLTAGE
VOLTAGE CONFIGURATION SIGNAL
CONTROL SIGNAL
FREQUENCY CONFIGURATION SIGNAL
FREQUENCY
126
112
128
110
124
122
VOLTAGE REGULATOR
CLOCK GENERATOR
120

FIGURE 1

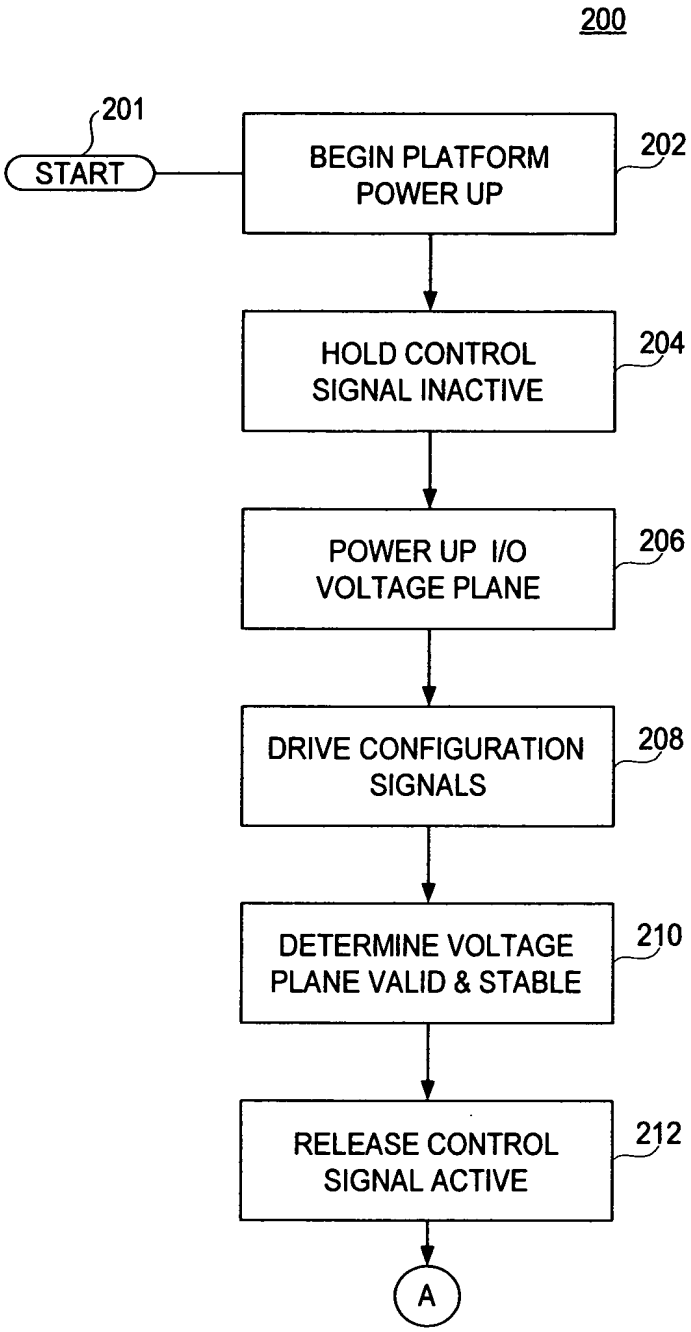
200
201
START
BEGIN PLATFORM POWER UP
202
HOLD CONTROL SIGNAL INACTIVE
204
POWER UP I/O VOLTAGE PLANE
206
DRIVE CONFIGURATION SIGNALS
208
DETERMINE VOLTAGE PLANE VALID & STABLE
210
RELEASE CONTROL SIGNAL ACTIVE
212
A

FIGURE 2A

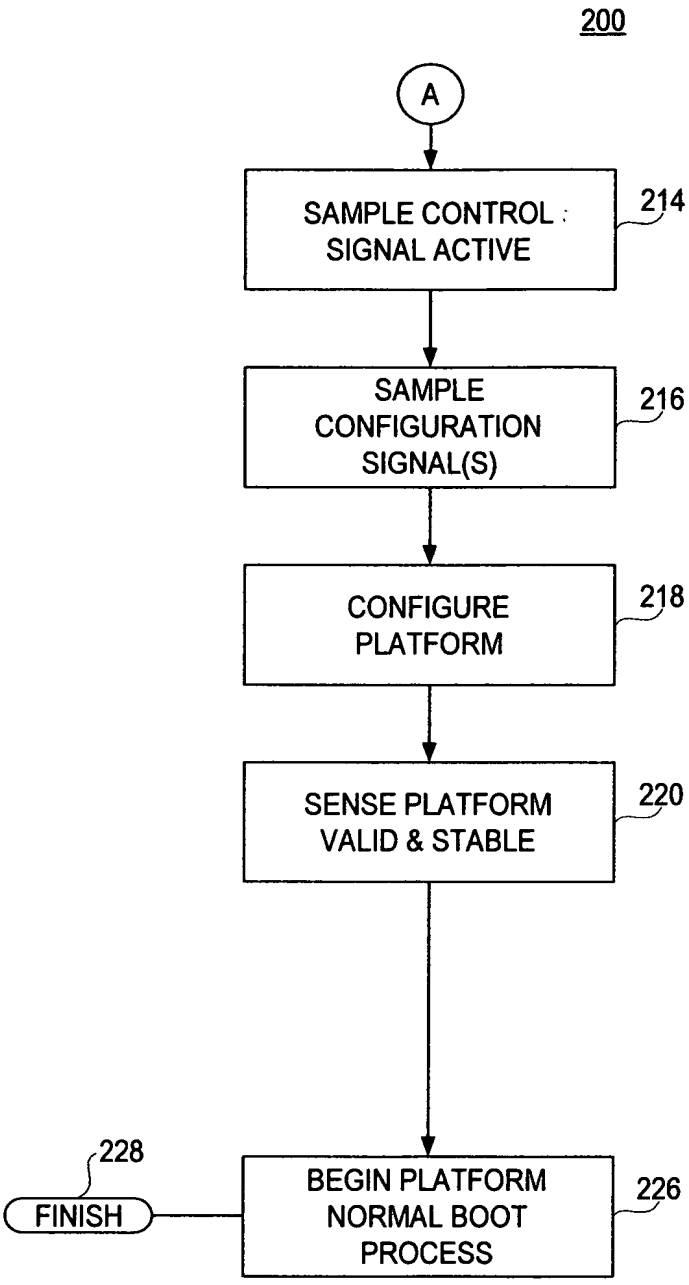
200
A
SAMPLE CONTROL SIGNAL ACTIVE
214
SAMPLE CONFIGURATION SIGNAL(S)
216
CONFIGURE PLATFORM
218
SENSE PLATFORM VALID & STABLE
220
228
FINISH
BEGIN PLATFORM NORMAL BOOT PROCESS
226

FIGURE 2B

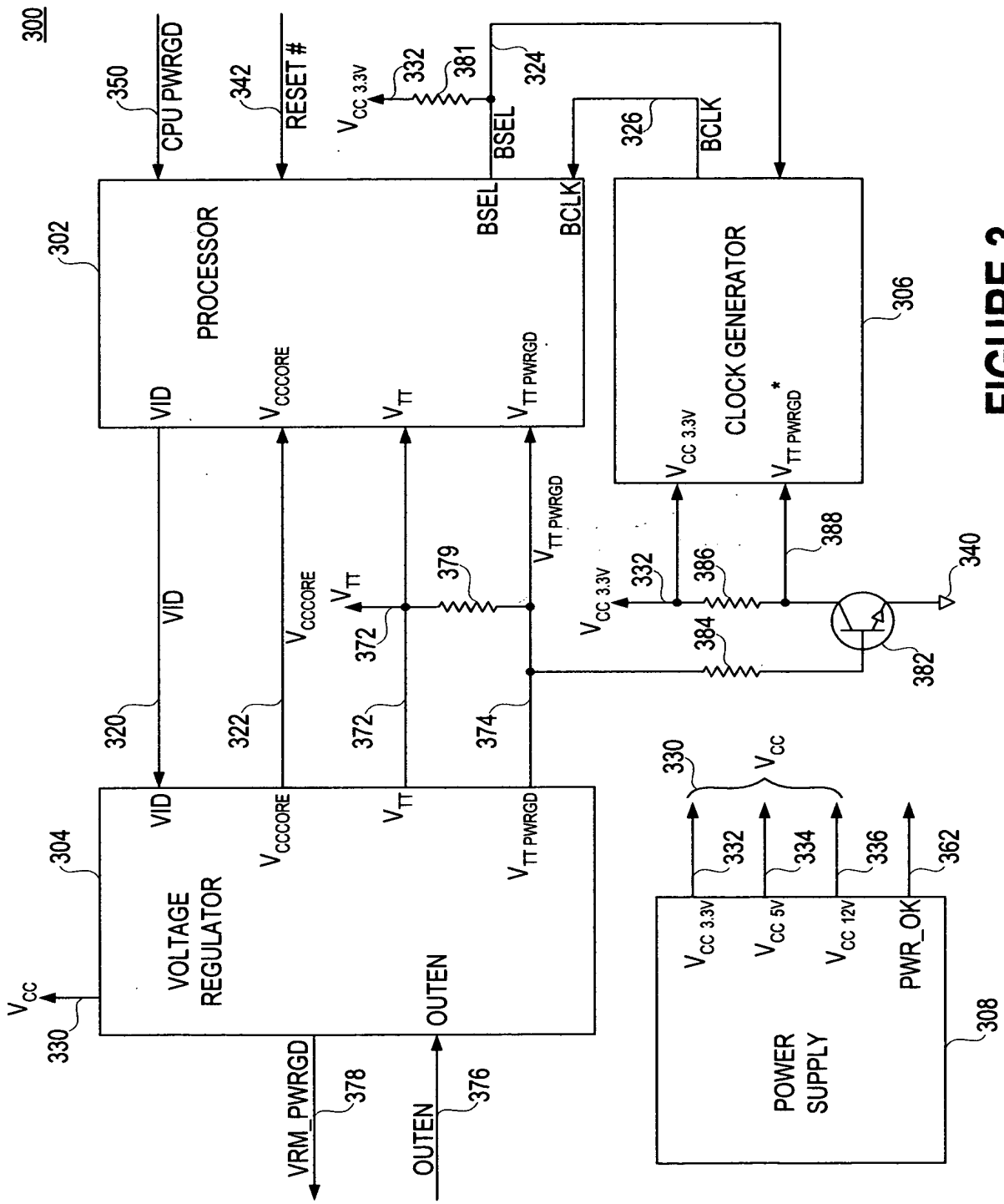
300
CPU PWRGD
350
RESET #
342
$V_{CC\ 3.3V}$
332
381
324
BSEL
BCLK
326
302
PROCESSOR
VID
V_{CCCORE}
V_{TT}
$V_{TT\ PWRGD}$
306
CLOCK GENERATOR
$V_{CC\ 3.3V}$
$V_{TT\ PWRGD}$ *
388
340
386
384
382
379
372
374
320
322
304
VOLTAGE REGULATOR
330
V_{CC}
VRM_PWRGD
378
OUTEN
376
POWER SUPPLY
$V_{CC\ 3.3V}$
$V_{CC\ 5V}$
$V_{CC\ 12V}$
PWR_OK
334
336
362
308

FIGURE 3

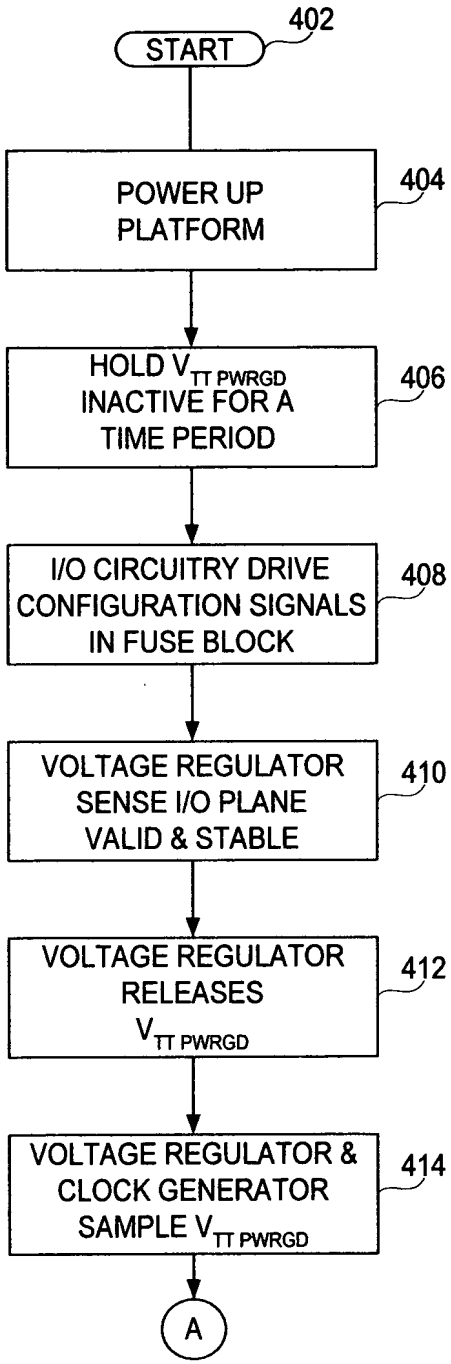
402
START
400
POWER UP PLATFORM
404
HOLD $V_{TT\ PWRGD}$ INACTIVE FOR A TIME PERIOD
406
I/O CIRCUITRY DRIVE CONFIGURATION SIGNALS IN FUSE BLOCK
408
VOLTAGE REGULATOR SENSE I/O PLANE VALID & STABLE
410
VOLTAGE REGULATOR RELEASES $V_{TT\ PWRGD}$
412
VOLTAGE REGULATOR & CLOCK GENERATOR SAMPLE $V_{TT\ PWRGD}$
414
A

FIGURE 4A

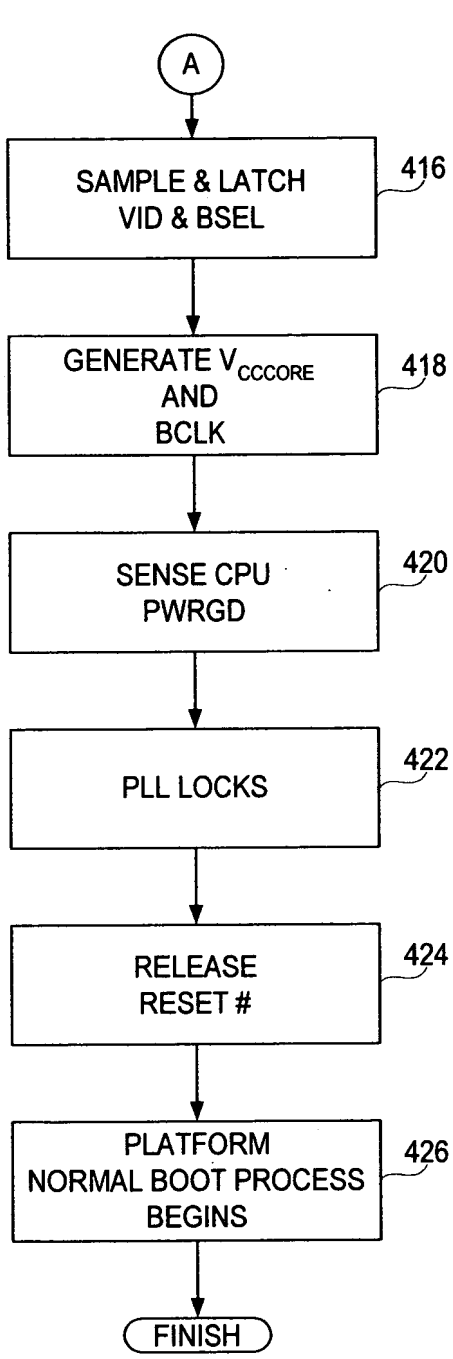
400
A
SAMPLE & LATCH VID & BSEL
416
GENERATE V_{CCCORE} AND BCLK
418
SENSE CPU PWRGD
420
PLL LOCKS
422
RELEASE RESET #
424
PLATFORM NORMAL BOOT PROCESS BEGINS
426
FINISH

FIGURE 4B

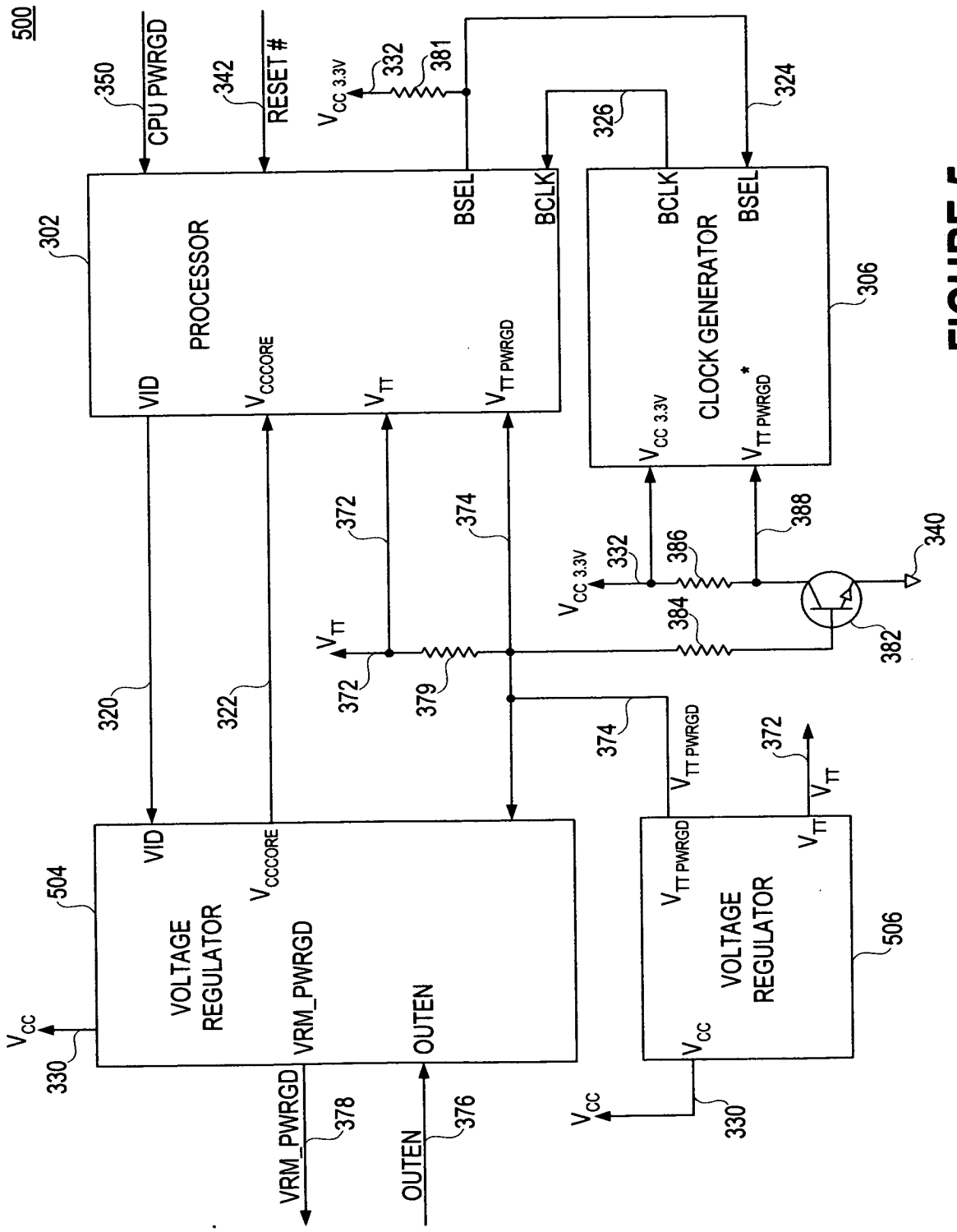
500
350
CPU PWRGD
342
RESET #
$V_{CC\ 3.3V}$
332
381
324
326
302
PROCESSOR
BSEL
BCLK
VID
V_{CCCORE}
V_{TT}
$V_{TT\ PWRGD}$
CLOCK GENERATOR
BCLK
BSEL
306
$V_{CC\ 3.3V}$
$V_{TT\ PWRGD}$ *
372
374
388
340
386
384
382
379
320
322
504
VOLTAGE REGULATOR
VID
V_{CCCORE}
VRM_PWRGD
OUTEN
V_{CC}
330
378
376
VRM_PWRGD
OUTEN
506
VOLTAGE REGULATOR
$V_{TT\ PWRGD}$
V_{TT}
V_{CC}
330

FIGURE 5

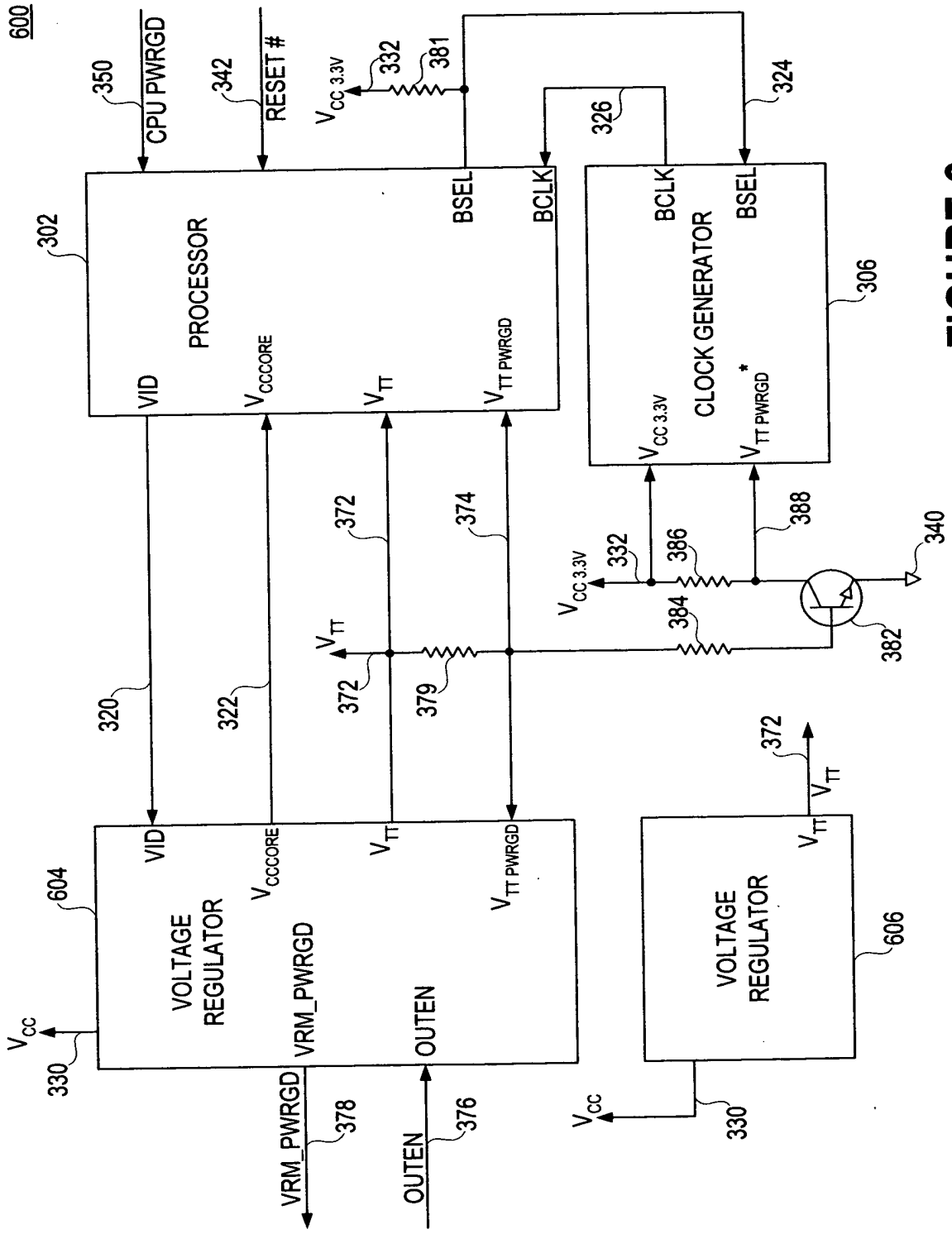
600
350
CPU PWRGD
342
RESET #
$V_{CC\ 3.3V}$
332
381
326
324
302
PROCESSOR
VID
V_{CCCORE}
V_{TT}
$V_{TT\ PWRGD}$
BSEL
BCLK
CLOCK GENERATOR
BCLK
BSEL
306
$V_{CC\ 3.3V}$
$V_{TT\ PWRGD}$ *
320
322
372
374
388
386
340
384
382
379
604
VOLTAGE REGULATOR
VID
V_{CCCORE}
V_{TT}
$V_{TT\ PWRGD}$
VRM_PWRGD
OUTEN
V_{CC}
330
VRM_PWRGD
378
OUTEN
376
606
VOLTAGE REGULATOR
V_{TT}
372
330

FIGURE 6

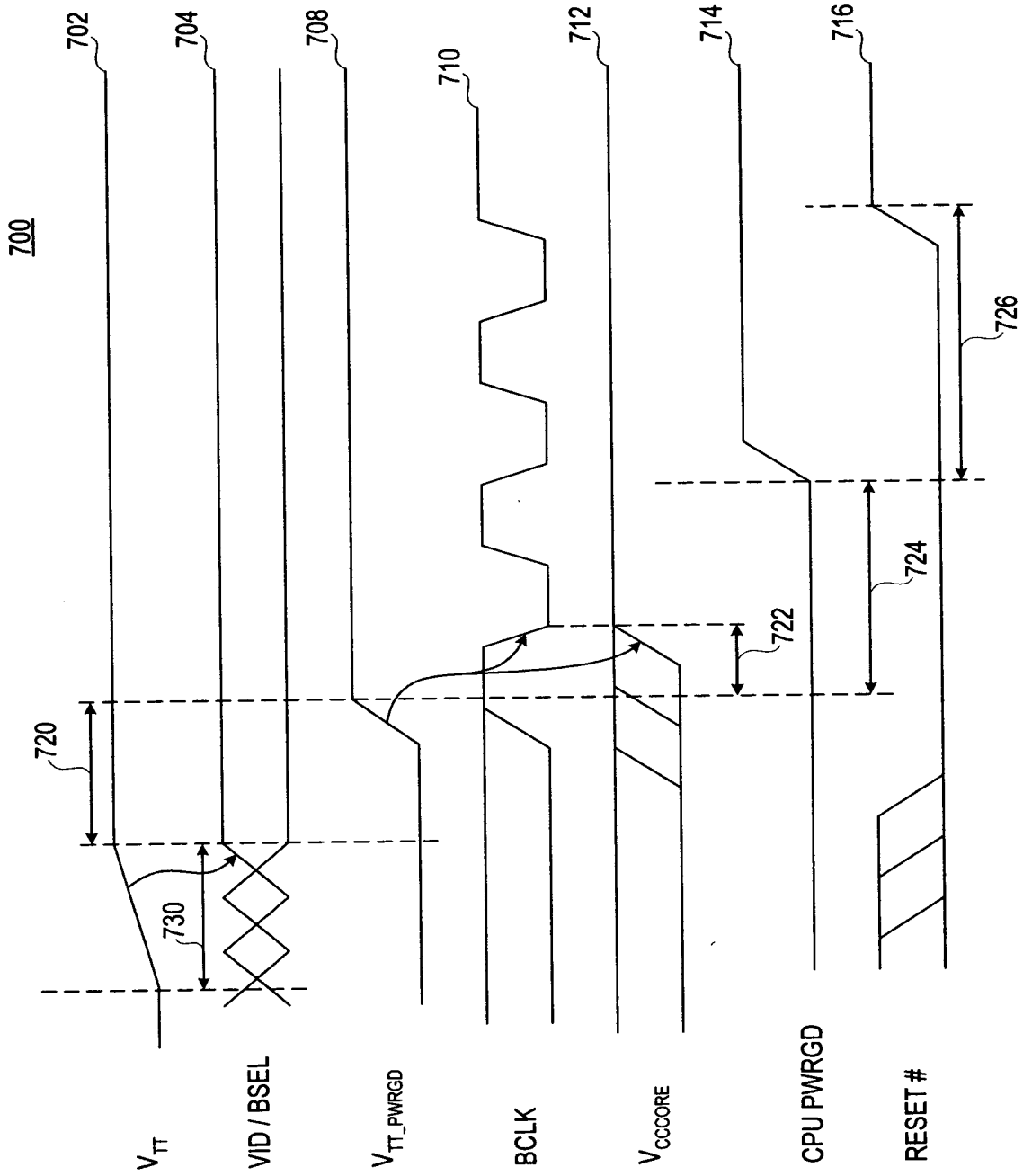
700
702
704
708
710
712
714
716
720
730
722
724
726
V_{TT}
VID / BSEL
V_{TT_PWRGD}
BCLK
V_{CCCORE}
CPU PWRGD
RESET #

FIGURE 7